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09/810,366	03/15/2001	Timothy B. Cowles	00-0058	9208

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ART UNIT	**PAPER NUMBER**
2133	7

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/810,366	COWLES, TIMOTHY B.
	Examiner	Art Unit
	Christine T. Tu	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 42-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 42-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/15/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3,4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. Claims 7-9, 42 and 47-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7:

At lines 1-3, the phrase "said act of tri-stating an output circuit ... comprising isolating said output circuit from a generally constant positive voltage source and from ground" cannot be understood.

Claim 42:

At line 4, the word "ship" should be replaced with –chip--.

Claim 47:

Throughout the claim, it is not clear what is the interrelationship among the output circuit with the memory array, the comparator or the address latch (except that "the output circuit comprising an inverter coupled to said memory array" is being recited at line 2). In other words, what exactly the output circuit is doing to the memory array.

Claims 8-9 and 48-49:

These claims are rejected because they depend on claim 7 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 10, 42-44 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashizume (6,259,639).

Claim 10:

Hashizume discloses the invention substantially as claimed. Hashizume teaches that a semiconductor integrated circuit device comprises a defective-memory-cell address holding register for latching a address as an defective address-memory-cell address (figure 1, column 7 line 44-46, column 8 line 11-18).

Claim 42:

Hashizume teaches that semiconductor integrated circuit device (figures 10 and 11) comprises a memory cell unit (10), an address latch (13) for receiving incoming address from outside the memory block, and a comparator (15) detects mismatch between the write data latched by the data latch (14) and the data read out of the test port of the memory cell unit (10) (figures 10 & 11, column 19 line 44-column 20 line 26).

Claims 43 and 44:

Hashizume also teaches that an address holding unit (15) includes a plurality of defective-memory-cell address holding registers (20) each for storing an address as a defective-memory-cell address when a mismatch is detected by the comparator (15) (figure 11, column 21 lines 2-11).

Claim 50:

Hashizume teaches (figure 15) a semiconductor integrated circuit device comprises a data processing unit for controlling a memory block (40). The memory block has the same structure as that as shown in FIG 1. The memory block (40) comprises use flags (44) and defective-memory-cell address registers (43). Hashizume also shows that when a comparator detects a mismatch between the original write data associated with an incoming address and corresponding data read out of the memory cell unit, the comparator determines that a memory cell into which the write data has been written is detective. Then, the holding unit (8) latches the defective address into

one of the plurality defective memory-cell address registers (43) and sets a corresponding one of the plurality of use flags (44) (figures15 & 1), column 25 lines 33-64).

Claim Rejections - 35 USC § 103

4. Claims 1-5, 11-28, 45-46 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (6,259,639).

Claims 1-5:

Hashizume discloses the invention substantially as claimed. Hashizume teaches (figures 15 & 1) a semiconductor integrated circuit device comprises plurality of memory blocks (40 & 41). Each memory block (40 & 41) has the same structure as that as shown in FIG 1. Each memory block comprises a memory cell unit (1), a redundant memory (2), an address latch (5) for receiving incoming address from outside the memory block, and a comparator (7) detects mismatch between the write data latched by the data latch (6) and the data read out of the test port of the memory cell unit (1). When a mismatch signal is output by the comparator (7), a defective memory cell address holding unit (8) latches a address as an defective address-memory-cell address. After that any access to the address will be made through the redundant memory (2) (figures 15 & 1, column 25, 16-21, column 7 line 1-column 8 line 19).

Hashizume does not explicitly teach the feature of preventing the stored bit from being output from the semiconductor chip. Hashizume suggests the feature of selecting [by a selector (9)] either data read out of the memory cell unit (1) or the write data

latched by the data latch (6) and for furnishing the selected data by the way of a data output terminal DO (column 7 lines 37-41).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to name Hashizume's selecting feature as a "preventing feature". The artisan would have been motivated to do so because such Hashimzume's selecting feature does prevent outputting the data being read from the memory cell unit when the time that the selector (9) selects the data from the latch (6).

Claim 11:

Hashizume does not explicitly teach that the defective-memory-cell address holding register is overwritten with the second address. Hashizume, however, teaches a plurality of defective-memory-cell address holding registers which can store later defective address when defective cell is determined later. It would have been obvious to one skilled in the art at the time the invention was made to realize that it would have a matter of design choice to use either a single address register or a plurality of registers (as taught by Hashizume). Such a choice would depend on the importance of keeping the prior stored addresses.

Claims 12-15:

Hashizume teaches that an address holding unit (15) includes a plurality of defective-memory-cell address holding registers (20) each for storing an address as a defective-memory-cell address when a mismatch is detected by the comparator (15).

Hashizume also teach a bit information register (21) for storing bits of write data in which a mismatch has been found by the comparator (15) (figures 10 & 11, column 21 lines 2-11, column 22 lines 18-31).

Hashizume further teaches that each correction flag (22) is set when the comparator (15) finds a mismatch and an address is stored in a corresponding defective-memory-cell address register (20) (figures 10 & 11, column 22 lines 31-37).

Claims 16-17:

Hashizume does not explicitly teach the feature of testing the semiconductor die after the act of rerouting. It would have been obvious to one skilled in the art to realize that continuously testing the semiconductor die after replacing a memory cell can be performed. The artisan would have been motivated to realize so because continuously testing the semiconductor die should be done until all memory cells in each semiconductor chips is being tested. In other words, the semiconductor die should be completely tested.

Claims 18-20:

Hashizume teaches (figure 1) a semiconductor integrated circuit comprising a memory cell unit (1) and a redundant memory (2). Any access to the defective address [that is being stored in a defective-memory-cell address holding unit (8)] will be made through the redundant unit (2). Hashizume also teaches the feature of replacing a

redundant memory cell of the redundant unit (2) for any future access of a defective address A (column 8 lines 11-19, column 9 line66-column 10 line 5).

Hashizume does not explicitly teach the replacement of a whole row or a whole column whenever a defective cell is found. It would have been a matter of design choice to replace either only a single redundant bit (as taught by hashizume), or to replace a whole redundant row/column when a defective cell is found. Such as choice would have depended on the availability of capacity in the redundant unit.

Claims 21-23:

Hashizume teaches that each correction flag (22) is set when the comparator (15) finds a mismatch and an address is stored in a corresponding defective-memory-cell address register (20) (figure 10, column 22 lines 31-37).

Hashizume further teaches that an address holding unit (15) includes a plurality of defective-memory-cell address holding registers (20) each for storing an address as a defective-memory-cell address when a mismatch is detected by the comparator (15). The mismatch is determined when a write data is not match with a corresponding data read out of a memory location by a comparison (figures 10 & 11, column 22 lines 20-27).

Claims 24-26:

Hashizume teaches the invention substantially as claimed. Hashizume teaches that memory cell unit (1) is being tested and repaired by testing the first address,

address A, and then the second address, address B, and then the third address, address C.... and so on (column 8 lines 56-column 10 line 58).

Hashizume does not explicitly teach the failing address found in the test result is an address not having been previously repaired. It would have been obvious to one skilled in the art at the time the invention was made that Hashizume's semiconductor integrated circuit device would comprise an address counter such that the address counter can activate the next address of a memory for testing when the testing present address the memory is done. The artisan would have been motivated to realize so because continuously testing the memory should be done until all memory cells within the memory is being tested. In other words, the whole memory should be completely tested.

Claim 27:

Hashizume teaches that each correction flag (22) is set when the comparator (15) finds a mismatch and an address is stored in a corresponding defective-memory-cell address register (20) (figure 10, column 22 lines 31-37).

Hashizume further teaches that an address holding unit (15) includes a plurality of defective-memory-cell address holding registers (20) each for storing an address as a defective-memory-cell address when a mismatch is detected by the comparator (15) (figures 10 & 11, column 22 lines 20-27).

Hashizume does not explicitly show that the register is configured to preferably store a latest defective address resulting from the test. Hashizume, however, teaches

that plurality of defective-memory-cell address registers (20) (figure 11) so that all defective addresses cam be stored the plurality of defective-memory-cell address registers (20). It would have been obvious to one skilled in the art at the time the invention was made to realize that it would have a matter of design choice to use either a single address register or a plurality of registers (as taught by Hashizume). Such a choice would depend on the importance of keeping the prior stored defective addresses.

Claim 28:

Hashizume teaches (figure 1) a semiconductor integrated circuit comprising a memory cell unit (1) and a redundant memory (2). Any access to the defective address [that is being stored in a defective-memory-cell address holding unit (8)] will be made through the redundant unit (2). Hashizume also teaches the feature of replacing a redundant memory cell of the redundant unit (2) for any future access of a defective address A (column 8 lines 11-19, column 9 line66-column 10 line 5).

Hashizume does not explicitly teach the replacement of a whole column whenever a defective cell is found. It would have been a matter of design choice to replace either only a single redundant bit (as taught by Hashizume), or to replace a whole redundant column when a defective cell is found. Such as choice would have depended on the availability of capacity in the redundant unit.

Claim 45:

Hashizume does not explicitly show that the register is configured to preferably store a later address corresponding to a later transmission of the signal over a prior address corresponding to a prior transmission of the signal. Hashizume, however, teaches that plurality of defective-memory-cell address registers (20) (figure 11) so that later a later address can be stored into another one of the plurality of defective-memory-cell address registers (20). It would have been obvious to one skilled in the art at the time the invention was made to realize that it would have a matter of design choice to use either a single address register or a plurality of registers (as taught by Hashizume). Such a choice would depend on the importance of keeping the prior stored addresses.

Claim 46:

Hashizume teaches that each correction flag (22) is set when the comparator (15) finds a mismatch and an address is stored in a corresponding defective-memory-cell address register (20) (figure 11, column 22 lines 31-37).

Claims 51;

Hashizume teaches not explicitly teach an anti-fuse bank configured to divert to a redundant memory cell. Hashizume also teaches a redundant unit (2) including plurality of cells, for taking the place of defective part of the memory cells disposed within the memory cell unit (10 to perform the function of the defective part (column 7 lines 7-10 and 41-42). It would have been obvious to one skilled in the art to realize that

Hashizume's invention would have been an anti-fuse bank to divert to a redundant memory cell. The artisan would have been motivated to realize so because Hashizume does teach that his invention is proposed to solve the problem of using a fuse-type memory repair technique (column 1 lines 43-47 and 33-40).

Claims 52-53:

Hashizume's semiconductor integrated circuit device can have two, three or more memory blocks each having the same structure as shown in FIGS 1, 4, 7, or 10, wherein such one of the memory blocks can be a random access memory cell unit (figures 15, column 25 lines 27-31 and lines 19-21, column 20 lines 46-51).

5. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (6,259,639) in view of Brown et al (5,946,246 and Brown hereinafter).

Claims 6 and 7:

Hashizume does not explicitly teach that the act of tri-stating an output circuit. However, Brown teaches a memory array test circuit including a three-state output buffer driver (118) for disabling data output in the event that a tri-state fail signal is output from a comparator (104) via a shift register (112) (figures 1, 18-19, column 3 lines 62-65).

It would have been obvious to one skilled in the art at the time the invention was made to use Brown's three-state buffer (118) instead of Hashizume's selector (9). The

artisan would have been motivated to do so because it is a matter of design choice whether to output a correct data or preventing any output when a mismatch is detected by a comparator.

Claim 8:

Hashizume teaches that write operation has to be done before the read operation (column 7 lines 56-63).

Claim 9:

Hashizume does not explicitly teach rewriting the test bit from the tester to the plurality of semiconductor chips. It would have been obvious to one skilled in the art to realize that continuously testing the semiconductor chips after replacing a memory cell can be performed. The artisan would have been motivated to realize so because continuously testing the semiconductor chips should be done until all memory cells in each semiconductor chips is being tested.

6. Claims 47-49 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (703)305-9689. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2133

June 27, 2004